NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

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Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

and invented by:

Christopher Morzano

If a CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [x] Filing fee as calculated and transmitted as described below
2. [x] Specification having 49 pages(s) and including the following:
   - a. [x] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [x] Background of the invention
   - f. [x] Brief summary of the invention
   - g. [x] Brief description of the drawings *(if drawings filed)*
   - h. [x] Detailed description
   - i. [x] Claims as classified below
   - j. [x] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal [X] Informal Number of sheets: 12

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	98	- 20 =	78	x $18.00	$1,404.00
Independent Claims	10	- 3 =	7	x $78.00	$546.00
Multiple Dependent Claims (check if applicable)			☐		
Other Fees (specify purpose): Recordation Form Cover Sheet					$40.00
				BASIC FEE	$760.00
				TOTAL FILING FEE	$2,750.00

☒ A check in the amount of $2,750.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 04-1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

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☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

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APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to integrated circuit chips and, in particular, to differential input buffers capable of reducing clock signal skew.

2. DESCRIPTION OF THE RELATED ART

Internal circuit functions in synchronous integrated circuits, e.g. SDRAM chips, are performed in response to transitions of an internal clock signal. Clock signals are signals that vary between a low voltage and a high voltage at regular intervals and are referenced to a fixed voltage, typically either the low voltage or the high voltage. The internal clock signal is derived from an external clock signal that has been passed through an input buffer as it enters the integrated circuit. The input buffer detects transitions in the external clock signal and outputs an internal clock signal, usually at a different reference voltage than the external clock signal.

Some circuits require differential input clock signals at a pair of terminals, i.e., signals that vary in opposed fashion. For example, delay stages in many delay-locked loops require high-speed, low-skew differential inputs for proper operation. Additionally, phase comparators in such delay-locked loops may also utilize differential input signals. Because integrated circuit devices that include

such delay-locked loops often receive only single-ended signals, the single-ended signals often must be converted to differential signals. Thus, the input buffer circuit may also produce complimentary internal clock signals where one signal follows the external clock signal, and the second signal follows the inverse of the external clock signal.

However, when a buffer circuit produces complimentary output signals, the output signals are susceptible to skew. For example, a first data signal generated and driven using a first internal clock signal is to be sampled by a second data signal driven by a second internal clock signal, the inverse of the first internal clock signal. If the two clock signals are skewed, e.g. they are out of phase with one another, then the first data signal may arrive too early or too late to be sampled by the second data signal. This situation is referred to as a "race condition" and is a result of excessive skew between two or more internal clock signals. Race conditions can cause an incorrect data value to be read when a data signal is sampled since the first data signal is not present when it is to be sampled. Therefore, race conditions can cause an integrated circuit to malfunction.

One approach to converting a single-ended signal into a differential signal is to run a single-ended external clock signal CLK through an inverter to produce an inverted signal CLK\. The noninverted and inverted signals CLK, CLK\ are then output at a pair of terminals as a differential signal. Because of the extra path length the inverted signal CLK\ travels, this signal arrives at the pair of terminals slightly after the noninverted signal CLK. The skew of the two signals

is typically on the order of 50 picoseconds or more, even with a very fast inverter. Such skew times are unacceptable for some applications, such as very low jitter delay locked loops and phase-locked loops. In such circuits, skewed input signals can cause instability, drift and jitter in the output signals.

The skew of signals CLK and CLK\ is illustrated in the timing diagram shown in Fig. 8. Signal CLK is low and signal CLK\ is high at time T1. At time T1, signal CLK transitions to a high state. Signal CLK\ begins to transition to a low state at time T2, the same time signal CLK reaches the end of its transition to a high state. At time T3, CLK reaches the end of its transition to a low state. The difference between T2 and T3 represents the skew of the signals CLK and CLK\.

In some cases the external clock signals arrive at an input buffer already in complimentary form. Fig. 9 illustrates in circuit diagram form a conventional differential input buffer circuit 200 used to produce and drive an internal clock signal CLK and inverse clock signal CLK\ from external clock signals XCLK and XCLK\, respectively. The circuit 200 generally comprises an input buffer 202 and a pair of clock driver circuits 204.

A typical input buffer 202 for use in a conventional differential input buffer circuit 200 is illustrated in circuit diagram form in Fig. 10. N-channel transistors 204 and 206 are connected to P-channel input transistors 208 and 210, respectively, to form a differential amplifier. The common source of P-

channel input transistors 208 and 210 is connected to voltage supply V_{CC} 212 through P-channel transistors 214 and 216. The common drain of N-channel input transistors 204 and 206 is connected to ground V_{SS} 218 through N-channel transistor 220. Clock signal CLK on line 222 is coupled to the gate of P-channel transistors 208 and 210 and N-channel transistors 204 and 206. N-channel transistors 226 and 228 are connected to P-channel transistors 230 and 232, respectively, to form a differential amplifier. The common source of P-channel transistors 230 and 232 is connected to positive voltage supply V_{CC} 212 through P-channel transistors 214 and 216. The common drain of N-channel input transistors 226 and 228 is connected to ground V_{SS} 218 through N-channel transistor 220. Clock signal CLK\ on line 224 is coupled to the gate of P-channel transistors 230 and 232 and N-channel transistors 226 and 228.

The output of the differential amplifiers at terminals 234 and 236 is coupled to the input of a pair of high threshold inverters formed by, respectively, P-channel transistors 238, 242, N-channel transistors 240, 244, voltage supplies 246, 250, and ground points 248, 252. The output of the high threshold inverters at terminals 254 and 256 provides internal clock signals CLK and CLK\.

In operation, when the enabling signal ENi is high, P-channel transistor 214 is off and N-channel transistors 258 and 260 are off due to the inversion of the signal ENi by inverter 262. When control signal ENi goes low,

P-channel transistor 214 is on, N-channel transistors 258 and 260 are on, and the differential amplifier is enabled.

When XCLK is high, P-channel transistors 208 and 210 are off and N-channel transistors 204 and 206 are on. Simultaneously, XCLK\ is low since it is the inverse of XCLK and P-channel transistors 230 and 232 are on and N-channel transistors 226 and 228 are off. Therefore, when XCLK is high and XCLK\ is low, terminal 234 is driven low, to V_{SS}, and terminal 236 is driven high, to V_{CC}. When terminal 234 is low, P-channel transistor 238 is on and N-channel transistor 240 is off, driving terminal 246 high, to V_{CC}. When terminal 236 is high, P-channel transistor 242 is off and N-channel transistor 244 is on, driving terminal 248 low, to V_{SS}. In comparison, when XCLK is low and XCLK\ is high, terminal 234 is high which drives terminal 246 low and terminal 236 is low which drives terminal 248 high.

While such a circuit buffers the external clock signals, it does not eliminate any pre-existing skew between the external clock signals. In addition, though it is useful for the regulated portion of an integrated circuit the resulting internal clock signals do not track well with the address and data inputs across the circuits operating voltage. Due to the large number and interdependence of transistors, the gate loading for this circuit leads to crossing point accuracy problems in response to fluctuations in voltage and temperature conditions.

Thus, there exists a need for a circuit to produce internal clock signals which exhibit less clock signal skew and which track well with address and data inputs, and are less susceptible to environmental conditions.

SUMMARY OF THE INVENTION

The present invention provides a clock signal input circuit that is able to provide inverse internal clock signals exhibiting reduced skew which are generated by the same input buffer as the address and data signals on an integrated circuit.

In a preferred embodiment, a skewed external noninverse clock signal and a corresponding external inverse clock signal are passed through respective reference voltage input buffers to produce internal clock signals. The internal clock signals are generated by the same input buffer as the address and data inputs. To reduce skew, back to back inverters are connected to both lines carrying the noninverted and inverted internal clock signals from the respective reference voltage input buffers. The slower internal clock signal has an extra inverter driving it when it switches states, e.g. from a high state to a low state, and the faster internal clock signal has an extra inverter fighting it when it switches states. The skew of the two signals is reduced, allowing for faster operation of the integrated circuit and a reduction in error in downstream circuits using the two signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will become more apparent from the detailed description of the preferred embodiments of the invention given below with reference to the accompanying drawings in which:

Fig. 1 is a block diagram of a clock skew reducing input buffer circuit of the present invention;

Fig. 2 is a schematic diagram of a reference voltage input buffer circuit shown in Fig. 1;

Fig. 3 is a schematic diagram of a clock skew reducing circuit shown in Fig. 1;

Fig. 4 is a timing diagram of the operation of the circuit of Fig. 3.

Fig. 5 is a schematic diagram of a driver circuit shown in Fig. 1;

Figs. 6a-d are timing diagrams of inverse clock signals undergoing a state transition.

Fig. 7 is a block diagram of a memory module employing the preferred embodiment of the present invention;

Fig. 8 is a timing diagram showing the skew between inverse clock signals.

Fig. 9 is a circuit schematic of a prior art differential input buffer circuit;

Fig. 10 is a circuit schematic of a prior art input buffer contained within the differential input buffer circuit of Fig. 9; and

Fig. 11 is a block diagram of a processor based system using the memory module of Fig. 7.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. Wherever possible, like numerals are used to refer to like elements and functions between the different embodiments of the present invention.

Fig. 1 shows a preferred embodiment of a circuit 5 of the present invention which buffers and drives incoming external clock signals CLK, CLK\ in addition to compensating for signal skew variations. The circuit 5 itself may be part of an integrated circuit which requires buffered internal clock signals exhibiting low skew, e.g. SDRAM chips.

The circuit 5 has at least two reference voltage input buffers 10, 11 each receiving an external clock signal XCLK and XCLK\ from lines 100, 101, respectively, a reference voltage signal V_{REF} from lines 102, 103, respectively, and an enable signal ENi from line 104. The reference voltage input buffers 10, 11 are each connected to clock skew reducer circuit 12 and drivers 14, 15 through lines 106, 107 respectively. Drivers 14 and 15 are preferably connected to any number of integrated circuit elements known in the art, e.g. a memory array 15.

A typical reference voltage input buffer 10 which may be used in the preferred embodiment of the invention is shown in Fig. 2. For the purposes of example, the input buffer 10 for the non-inverse external clock signal XCLK is shown, though the input buffer 11 for the inverse clock signal XCLK\ is identical in structure and operation. N-channel transistors 18 and 20 are connected to P-channel input transistors 22 and 24, respectively, to form a differential amplifier 25. The common source of P-channel transistors 22 and 24 is connected to voltage supply (V_{CC}) 26 through P-channel transistors 28 and 30. V_{CC} 26 is the internal voltage of the circuit 5. The common source of N-channel input transistors 18 and 20 is connected to ground (V_{SS}) 32 through N-channel transistor 34. Reference signal V_{REF} on line 102 is coupled to the gate of P-channel input transistor 22 and N-channel transistor 18. V_{REF} is preferably the reference voltage for the address and data signal inputs of the integrated circuit of which circuit 5 is a portion thereof. The external clock signal XCLK on line 100 is coupled to the gate of P-channel transistor 24 and N-channel transistor 20. The output of the differential amplifier 25 at terminal 36 is coupled to the

input of a high threshold inverter 37 formed by P-channel transistor 38 and N-channel transistors 40 and 42. The output of the high threshold inverter 37 at terminal 44 is internal clock signal CLK and is output on line 106. Though one particular type of reference voltage input buffer 10 has been described herein, it should be understood that any reference voltage input buffer known in the art may be substituted. In addition, any differential input buffer known in the art may also be substituted for reference voltage input buffer 10.

Input buffer 11 is preferably identical in operation and construction to input buffer 11, described above, though it may be any buffer circuit capable of buffering an external clock signal to an internal voltage supply (Vcc). Similar to input buffer 10, the input buffer 11 receives the external inverse clock signal XCLK\ and buffers the signal to produce an output which is the internal inverse clock signal CLK\.

In operation, when the enabling signal ENi is high, P-channel transistor 28 is off and N-channel transistor 42 is on. Thus, the differential amplifier 25 is disabled, terminal 36 of the differential amplifier 25 is low, terminal 44 of the high threshold inverter 37 is high, and, therefore, CLK is held high. When control signal ENi goes low, P-channel transistor 28 is on, N-channel transistor 42 is off, and the differential amplifier 25 is enabled. XCLK is then compared with reference signal V_{REF} by P-channel transistors 22 and 24. If XCLK is in a high state, having a voltage greater than reference signal V_{REF}, P-channel input transistor 24 is less conductive than P-channel input transistor 22

and the output at terminal 36 goes low. This causes transistor 38 to become more conductive, thus driving terminal 44 high to V_{CC}. If XCLK is in a low state, having a lower voltage than reference signal V_{REF}, terminal 36 will be driven high, making N-channel transition 40 more conductive and driving terminal 44 low, to ground. This results in CLK on line 106 being held in a low state.

When the input buffers 10, 11, as shown in Fig. 1, are operating to buffer respective incoming signals XCLK and XCLK\, they provide internal clock signals CLK and CLK\ on respective lines 106, 107. The input buffer 10 for incoming signal XCLK will latch when XCLK crosses V_{REF}, the threshold voltage. Similarly, the input buffer 11 for incoming signal XCLK\ will latch when XCLK\ crosses V_{REF}. With the use of the relatively low transistor-count reference voltage input buffers 10, 11, the dependence of the circuit 5 on adverse environmental conditions is decreased. This is a benefit since adverse environmental conditions, e.g. high temperatures, can lead to a greater chance of skew and race conditions. However, specifications for synchronous circuits base clock transitions upon the crossing point of CLK and CLK\. The input buffers 10, 11 do not reduce the skew between the CLK and CLK\ signals. To accomplish a reduction in skew, a clock skew reducing circuit 12 is connected to CLK and CLK\ output lines 106, 107 as shown in Figs. 1 and 2.

The clock skew reducing circuit 12 is shown in more detail in Fig. 3. N-channel transistors 50 and 52 are connected to P-channel transistors 54 and 56, respectively, to form a pair of back-to-back inverters. The common source of P-channel transistors 54 and 56 is connected to voltage supply (V_{CC})58, which is preferably the same voltage supply as V_{CC} 26, through P-channel transistor 60, gated by enable signal ENi on line 104. The common source of N-channel transistors 50 and 52 is connected to ground (V_{SS})62 through N-channel transistor 64, gated by enable signal ENi on line 104 which has been driven through inverter 66.

The CLK signal on line 106 is coupled to the gate of P-channel transistor 56 and N-channel transistor 52, the drain of P-channel transistor 54, and the source of N-channel transistor 50. The signal CLK\ on line 107 is coupled to the gate of P-channel transistor 54 and N-channel transistor 50, the drain of P-channel transistor 56, and the source of N-channel transistor 52. In operation, when the enabling signal ENi is high, P-channel transistor 60 is off and N-channel transistor 64 is off. Thus, the clock skew reducing circuit 10 is disabled. When control signal ENi goes low, P-channel transistor 60 is on and N-channel transistor 64 is on which enables the clock skew reducing circuit 12.

To reduce skew between the signals CLK and CLK\, the clock skew reducing circuit 12 drives the slower signal and inhibits the faster signal in the following manner. When two signals are skewed, one is considered "faster" than

the other. The term "faster" refers to a comparison of the points in time at which the two signals reach a transition, e.g. crossing V_{REF}. For example, if signal CLK is faster than signal CLK\, signal CLK will transition, e.g., from a low to high state, before CLK\ transitions, e.g., from a high to low state. Thus, if CLK transitions to a high state, P-channel transistor 56 becomes less conductive and N-channel transistor 52 becomes more conductive than when CLK was in a low state. Simultaneously, CLK\, because it is slower, is still high and P-channel transistor 54 has a lower conductivity than N-channel transistor 50. Therefore, signal CLK's path through transistors 54, 56, 52, and 50 will be slower than signal CLK\'s path through transistors 52, 50, 54, and 56. The transition of the first signal, signal CLK in this example, is slower than the transition of the slow signal, CLK\. A similar operation occurs if CLK\ is faster than CLK with CLK\ being slowed. The output signals CLK and CLK\ on terminals 68 and 79, respectively, exhibit reduced skew due to the use of the skew reducing circuit 12.

More particularly, operation of the clock skew reducing circuit 12 is illustrated in the timing diagram shown in Fig. 4. We again assume for discussion that CLK is faster than CLK\. Signal CLK is low and signal CLK\ is high at time T_1 as both signals enter the clock skew reducing circuit 12. A brief period after T_1, at time T_2, signal CLK transitions to a high state. Signal CLK\ begins to transition to a low state at time T_3. The difference between T_2 and T_3 represents the skew of the signals CLK and CLK\ prior to entering the clock skew reduction circuit 12. However, skew reducing circuit 12 causes both

signals CLK and CLK\ to finish their respective transitions at the same time, T_4. Even though both signals CLK and CLK\ began their transitions with a skew, the operation of the clock skew reducing circuit 12 has greatly reduced or eliminated the skew by slowing the transition of signal CLK, the fast signal, and speeding the transition of signal CLK\, the slow signal. Alternatively, if signal CLK\ is fast and signal CLK is slow, the clock speed reducing circuit 12 will slow the transition of signal CLK\ and speed the transition of signal CLK.

Before being transmitted from the circuit 5, the signals CLK and CLK\ are preferably passed through driver circuits 14 and 15, respectively, to boost signal strength. A typical driver circuit 14 is shown in more detail in Fig. 5. Incoming clock signal CLK is passed through a series of at least two inverters 72 and 74 to terminal 76. The inverters 72 and 74 strengthen the signal CLK. More preferably, the driver circuit 14 has a third inverter 78 which outputs a signal that gates N-channel transistor 80. The drain for N-channel transistor 80 is ground (V_{SS}) 82 and the source is the output of inverter 74. In operation, when the signal CLK is high, the N-channel transistor 80 is in an off state and the boosted signal CLK at terminal 76 is output on line 108. When the signal CLK is low, the N-channel transistor 80 is in an on state and the boosted signal CLK at terminal 76 is driven to ground by V_{SS} 82. Though one particular type of driver circuit 14 has been described herein, it should be understood that any driver circuit known in the art may be substituted.

To demonstrate the reduction in skew produced by the present invention, two circuits were simulated across four conditions of clock skew. Circuit A was a prior art differential input buffer as shown in Figs. 9 and 10 and described above and Circuit B was a circuit as depicted in Figs. 1 and 2 and constructed in accordance with the present invention. The four skew conditions are shown in Figs. 6a, 6b, 6c, and 6d. Fig. 6a shows signal XCLK transitioning from a low state to a high state, XCLK\ transitioning from a high state to a low state, V_{REF} equal to 1.15 V, and a 200 ps skew between signals XCLK and XCLK\ crossing V_{REF} with signal XCLK crossing V_{REF} first, thus being the fast signal. Fig. 6b shows a similar condition with signal XCLK\ being fast and signal XCLK being slow. Fig. 6c shows signal XCLK transitioning from a low state to a high state, XCLK\ transitioning from a high state to a low state, V_{REF} equal to 1.35 V, and a 200 ps skew between signals XCLK, the fast signal, and XCLK\, the slow signal, crossing V_{REF}. Fig. 6d shows a similar condition with signal XCLK\ being fast and signal XCLK being slow. To test Circuit A and Circuit B, a transmitted data/address signal crossed V_{REF} at the same time that signals XCLK and XCLK\ intersected V_{REF}. The time difference between the data/address signal crossing V_{REF} and the signal XCLK crossing V_{REF} were measured, the results shown in Table 1 below.

Environmental Conditions	Worst Case Skew Difference		Skew Difference Worst To Best	
	A picoseconds (ps)	B (ps)	A (ps)	B (ps)
V_{CC} = 2.2; Temperature = 85 F	780	130	470	120
V_{CC} = 2.2; Temperature = 85 F	156	116	40	114
Across V_{CC} and Temperature	780	130	660	130

A can be seen from the results in Table 1, the invention, Circuit B, saved up to 0.5 ns of the setup/hold window for data/address signals over prior art Circuit A.

The invention is particularly useful in an integrated memory circuit. In particular, the input buffer is useful in memory devices, for example in a double data rate synchronous dynamic random access memory (DDR SDRAM). Typically DDR SDRAM chips employ a delay on address signals to compensate for the skew in clock signals. Such a delay could be eliminated through use of the present invention. A simplified block diagram of an DDR SDRAM 72 is illustrated in Fig. 7. The DDR SDRAM 72 includes an array of memory cells 74, address circuitry 76 for addressing the memory array, clock skew reducing circuit 5, input/output (I/O) buffer circuitry 80 for data input and output, and control circuitry 78 for controlling the operation of the DDR SDRAM 72. The circuit 5 includes at least the input buffer 10, clock skew reducing circuit 12, and driver circuits 14 described above and shown in Figs. 1-4. Also shown in Fig. 7 is an external processor 82, preferably a microprocessor, which is typically used to access memory 72 provide control signals on lines 110, address signals on lines 112, input/output data on lines 114, and clock signals CLK and CLK\ on lines 100, 101, respectively. It will be appreciated by those skilled in the art that the DDR SDRAM of Fig. 7 is simplified to illustrate the present invention and is not intended to be a detailed description of all of the features of an DDR SDRAM.

The processor 82 and memory 72 may form part of a layer general purpose computing system as shown in Fig. 11. Fig. 11 is a block diagram of a processor-based system 150 utilizing a memory 72 constructed in accordance with one of the embodiments of the present invention. The processor-based system 150 may be a computer system, a process control system or any other system employing a processor and associated memory. The system 150 includes a processor 82, e.g., a microprocessor, that communicates with the memory 72 and an I/O device 116 over a bus 118. It must be noted that the bus 118 may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus 118 has been illustrated as a single bus. A second I/O device 120 is illustrated, but is not necessary to practice the invention. The processor-based system 150 also includes read-only memory (ROM) 122 and may include peripheral devices such as a floppy disk drive 124 and a compact disk (CD) ROM drive 126 that also communicates with the CPU 82 over the bus 118 as is well known in the art.

Although the invention has been described with reference to SDRAMS, such as regulated DDR SDRAMS, the invention has broader applicability and may be used in many integrated circuit applications. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A circuit for reducing signal skew comprising:

at least a first and second signal input/output line for receiving first and second input signals and transmitting first and second output signals; and

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second signal input/output line.

2. The circuit of claim 1 further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second inverters in response to the enable signal.

3. The circuit of claim 2, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being gated to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being gated to said first and second inverters by the inverted enable signal.

4. The circuit of claim 3, wherein said first voltage source is gated by a P-channel transistor responsive to the enable signal.

5. The circuit of claim 3, wherein said second voltage source is gated by a N-channel transistor responsive to the inverse of the enable signal.

6. The circuit of claim 3, wherein said first voltage source is gated by an N-channel transistor responsive to the enable signal.

7. The circuit of claim 3, wherein said second voltage source is gated by an P-channel transistor responsive to the inverse of the enable signal.

8. The circuit of claim 1, further comprising first and second input buffer circuits for receiving first and second external signals.

9. The circuit of claim 8, wherein each of said first and second input buffer circuits comprises:

an input for receiving an external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

10. The circuit of claim 9, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

11. The circuit of claim 1, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

12. The circuit of claim 11, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

13. The circuit of claim 12, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

14. The circuit of claim 1, wherein each of said first and second inverters are comprised of series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to respective of said input/output lines.

15. The circuit of claim 14, wherein said first and second inverters include:

a first N-channel transistor coupled in parallel to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled in parallel to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

16. A circuit for reducing clock signal skew comprising:

at least a first and second clock signal input/output line for receiving first and second clock input signals and transmitting first and second internal clock signals;

a first N-channel transistor coupled in parallel to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled in parallel to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

said first N-channel transistor coupled in series to said first P-channel transistor and said second signal input/output line connected between said first N-channel transistor and said first P-channel transistor.

17. The circuit of claim 16, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second N-channel transistors and said first and second P-channel transistors in response to the enable signal.

18. The circuit of claim 17, wherein said enable circuit comprises:

a third P-channel transistor having a source coupled to a voltage supply, a gate coupled to receive the enable signal, and a drain coupled to a source of said first and second P-channel transistors;

an enable inverter for inverting the enable signal; and

a third N-channel transistor having a drain coupled to a ground, a gate coupled to receive the inverted enable signal, and a drain coupled to a drain of said first and second N-channel transistors.

19. The circuit of claim 17, wherein said enable circuit comprises:

a third N-channel transistor having a source coupled to a voltage supply, a gate coupled to receive the enable signal, and a drain coupled to a source of said first and second N-channel transistors;

an enable inverter for inverting the enable signal; and

a third P-channel transistor having a drain coupled to a ground, a gate coupled to receive the inverted enable signal, and a drain coupled to a drain of said first and second P-channel transistors.

20. The circuit of claim 16, further comprising first and second input buffer circuits for receiving first and second external signals.

21. The circuit of claim 20, wherein each of said first and second input buffer circuits comprises:

an input for receiving an external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

22. The circuit of claim 21, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

23. The circuit of claim 16, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

24. The circuit of claim 23, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

25. The circuit of claim 24, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

26. A circuit for reducing signal skew comprising:

at least a first and second signal input/output line for receiving first and second input signals and transmitting first and second output signals;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second signal input/output line; and

a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

27. The circuit of claim 26, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second inverters in response to the enable signal.

28. The circuit of claim 27, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being gated to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being gated to said inverters by the inverted enable signal.

29. The circuit of claim 28, wherein said first voltage source is gated by a P-channel transistor responsive to the enable signal.

30. The circuit of claim 28, wherein said second voltage source is gated by a N-channel transistor responsive to the inverse of the enable signal.

31. The circuit of claim 8, wherein said first voltage source is gated by an N-channel transistor responsive to the enable signal.

32. The circuit of claim 8, wherein said second voltage source is gated by an P-channel transistor responsive to the inverse of the enable signal.

33. The circuit of claim 26, further comprising first and second input buffer circuits for receiving first and second external signals.

34. The circuit of claim 33, wherein each of said first and second input buffer circuits comprises:

an input for receiving an external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal

when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

35. The circuit of claim 34, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

36. The circuit of claim 26, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

37. The circuit of claim 36, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

38. A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving an external clock signal;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

39. The circuit of claim 38, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

40. The circuit of claim 39, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being gated to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being gated to said inverters by the inverted enable signal.

41. The circuit of claim 40, wherein said first voltage source is gated by a P-channel transistor responsive to the enable signal.

42. The circuit of claim 40, wherein said second voltage source is gated by a N-channel transistor responsive to the inverse of the enable signal.

43. The circuit of claim 40, wherein said first voltage source is gated by an N-channel transistor responsive to the enable signal.

44. The circuit of claim 40, wherein said second voltage source is gated by an P-channel transistor responsive to the inverse of the enable signal.

45. The circuit of claim 38, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

46. The circuit of claim 45, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

47. The circuit of claim 46, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

48. A circuit for buffering a clock signal comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving an external clock signal;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line; and

a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

49. The circuit of claim 48, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuit and said second and third inverters in response to the enable signal.

50. The circuit of claim 49, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said second inverter and said third inverter, said first voltage supply being gated to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said third inverter and said second inverter, said second voltage source being gated to said inverters by the inverted enable signal.

51. The circuit of claim 50, wherein said first voltage source is gated by a P-channel transistor responsive to the enable signal.

52. The circuit of claim 50, wherein said second voltage source is gated by a N-channel transistor responsive to the inverse of the enable signal.

53. The circuit of claim 50, wherein said first voltage source is gated by an N-channel transistor responsive to the enable signal.

54. The circuit of claim 50, wherein said second voltage source is gated by an P-channel transistor responsive to the inverse of the enable signal.

55. The circuit of claim 48, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

56. The circuit of claim 55, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

57. A synchronous memory device comprising:

an array of memory cells;

at least one clock input for receiving at least one clock signal and for producing first and second internal clock signals; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least first and second inverters each having an input and an output, said input of said first inverter connected to said output of said

second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line.

58. The synchronous memory device of claim 57, wherein said circuit for reducing skew further comprises an enable circuit for receiving an enable signal and enabling or disabling said first and second inverters in response to the enable signal.

59. The synchronous memory device of claim 58, wherein said enable circuit comprises:

a first voltage source for supply of a first voltage to said first inverter and said second inverter, said first voltage supply being gated to said inverters by the enable signal;

an enable inverter for inverting the enabling signal;

a second voltage source for supplying a second voltage to said second inverter and said first inverter, said second voltage source being gated to said first and second inverters by the inverted enable signal.

60. The synchronous memory device of claim 59, wherein said first voltage source is gated by a P-channel transistor responsive to the enable signal.

61. The synchronous memory device of claim 59, wherein said second voltage source is gated by a N-channel transistor responsive to the inverse of the enable signal.

62. The synchronous memory device of claim 59, wherein said first voltage source is gated by an N-channel transistor responsive to the enable signal.

63. The synchronous memory device of claim 59, wherein said second voltage source is gated by an P-channel transistor responsive to the inverse of the enable signal.

64. The synchronous memory device of claim 57, further comprising first and second input buffer circuits for receiving first and second external signals.

65. The synchronous memory device of claim 64, wherein each of said first and second input buffer circuits comprises:

an input for receiving an external signal;

an input for receiving a reference voltage signal;

a differential amplifier coupled to said input, said differential amplifier having an output terminal for providing a latch signal in response to the external signal in comparison to the reference voltage signal, the latch signal having a first or second state;

a buffer circuit inverter connected to said output terminal of said differential amplifier, said buffer circuit inverter generating a first internal signal

when the latch signal is in a first state, and a second internal signal when the latch signal is in a second state; and

an input line for transmitting said first or second internal signal, said input line connected to one of said first and second signal input/output lines.

66. The synchronous memory device of claim 65, further comprising an enable circuit for receiving said enable signal and enabling or disabling said first and second input buffer circuits in response to the enable signal.

67. The synchronous memory device of claim 57, further comprising a first and second driver circuit for boosting said output signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

68. The synchronous memory device of claim 67, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

69. The synchronous memory device of claim 68, further comprising at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to a predetermined voltage.

70. A synchronous memory device comprising:

an array of memory cells;

a clock input for receiving a clock signal; and

a clock input buffer comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving an external clock signal;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

71. The synchronous memory device of claim 70, wherein the memory device is a synchronous dynamic random access memory (SDRAM).

72. The synchronous memory device of claim 70, further comprising an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuits and said second and third inverters in response to the enable signal.

73. The synchronous memory device of claim 70, further comprising a first and second driver circuit for boosting said internal clock signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

74. The synchronous memory device of claim 73, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

75. The synchronous memory device of claim 73, wherein at least one of said first and second driver circuits comprises at least first and second driver inverters connected in series and at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to ground.

76. A computer system comprising:

a processor;

a memory circuit connected to said processor, said memory circuit comprising:

an array of memory cells;

a clock input for receiving a clock signal; and

a clock input buffer comprising:

a first and second input buffer circuit for receiving a first and second external clock signal, respectively, each of said input buffer circuits comprising:

an input for receiving an external clock signal;

a differential amplifier coupled to the input, said differential amplifier having an output terminal for providing a latch signal in response to the external clock signal, the latch signal having a first or second state; and

a first inverter connected to said output terminal, said first inverter generating an internal clock signal in response to the latch signal, said first inverter generating a first internal clock signal when the latch signal is in a first state, and a second internal clock signal when the latch signal is in a second state; and

a circuit for reducing skew between the first and second internal clock signals, said circuit comprising:

first and second clock signal input/output lines for receiving and transmitting first and second internal clock signals, respectively; and

at least second and third inverters each having an input and an output, said input of said second inverter connected to said output of said third inverter and to said first clock signal input/output line and said input of said third inverter connected to said output of said second inverter and to said second clock signal input/output line.

77. The computer system of claim 76, wherein said memory circuit is a synchronous dynamic random access memory (SDRAM).

78. The computer system of claim 76, wherein said memory circuit further comprises an enable circuit for receiving an enable signal and enabling or disabling said first and second input buffer circuits and said second and third inverters in response to the enable signal.

79. The computer system of claim 76, wherein said memory circuit further comprises a first and second driver circuit for boosting said internal clock signal, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

80. The computer system of claim 79, wherein at least one of said first and second driver circuits comprises at least a first and second driver inverter connected in series.

81. The computer system of claim 79, wherein at least one of said first and second driver circuits comprises at least first and second driver inverters connected in series and at least a third driver inverter connected in parallel to said first and second driver inverters, the output of said third driver inverter gating the output of said first and second driver inverters to ground.

82. A method of generating an internal clock signal in an integrated circuit, the method comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag of one of said external clock signals relative to the other; and

modifying the transition of one of said external clock signals relative to the other to produce from said external clock signals internal clock signals which have reduced skew.

83. The method of claim 82, further comprising the step of buffering each of the first and second external clock signals using a reference voltage.

84. The method of claim 83, wherein said step of modifying the transition of one of said buffered external clock signals comprises the step of transmitting each of said buffered external clock signals through series connected complimentary transistors, the respective connection terminal of said series connected complimentary transistors being coupled to respective input/output lines for receiving said first and second external clock signals.

85. The method of claim 83, wherein said step of modifying the transition of one of said buffered external clock signals comprises the steps of:

speeding the transition of said buffered external clock signal having a time lag; and

slowing the transition of the other of said buffered external clock signals.

86. The method of claim 82, further comprising the step of driving each of said internal clock signals.

87. The method of claim 82,, wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.

88. The method as in claim 87, wherein said random access memory comprises a dynamic random access memory.

89. The method of claim 82, further comprising transmitting said internal clock signals to a memory circuit.

90. The method as in claim 89, wherein said memory circuit comprises a dynamic random access memory.

91. A method of generating an internal clock signal in an integrated circuit, the method comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag of one of said external clock signals relative to the other;

buffering each of the first and second external clock signals using a reference voltage;

modifying the transition of one of said buffered external clock signals relative to the other to produce from said buffered external clock signals internal clock signals which have reduced skew.

92. The method of claim 91, wherein said step of modifying the transition of one of said buffered external clock signals comprises the steps of:

speeding the transition of said buffered external clock signal having a time lag; and

slowing the transition of the other of said buffered external clock signals.

93. The method of claim 91, wherein said step of modifying the transition of one of said buffered external clock signals comprises the step of transmitting each of said buffered external clock signals through series connected complimentary transistors, the

respective connection terminal of said series connected complimentary transistors being coupled to respective input/output lines for receiving said first and second external clock signals.

94. The method of claim 91, further comprising the step of driving each of said internal clock signals.

95. The method of claim 91, wherein said act of receiving first and second external clock signals is performed in connection with the operation of a random access memory.

96. The method of claim 94, wherein said random access memory comprises a dynamic random access memory.

97. The method of claim 91, further comprising transmitting said internal clock signals to a memory circuit.

98. The method as in claim 96, wherein said memory circuit comprises a dynamic random access memory.

ABSTRACT

The present invention provides a clock signal input circuit that is able to provide inverse internal clock signals generated by the same input buffer as the address and data signals which exhibit reduced skew. When a skewed external noninverse clock signal and a corresponding external inverse clock signal are passed through respective reference voltage input buffers there is no reduction in skew between the two internal signals. In a preferred embodiment, the invention provides back to back inverters connected to both lines carrying the noninverted and inverted internal clock signals. The slower internal clock signal has an extra inverter driving it when it switches states and the faster internal clock signal has an extra inverter fighting it when it switches states. The skew of the two signals is reduced, allowing for faster operation of the integrated circuit and a reduction in misread data signals.

Fig. 1

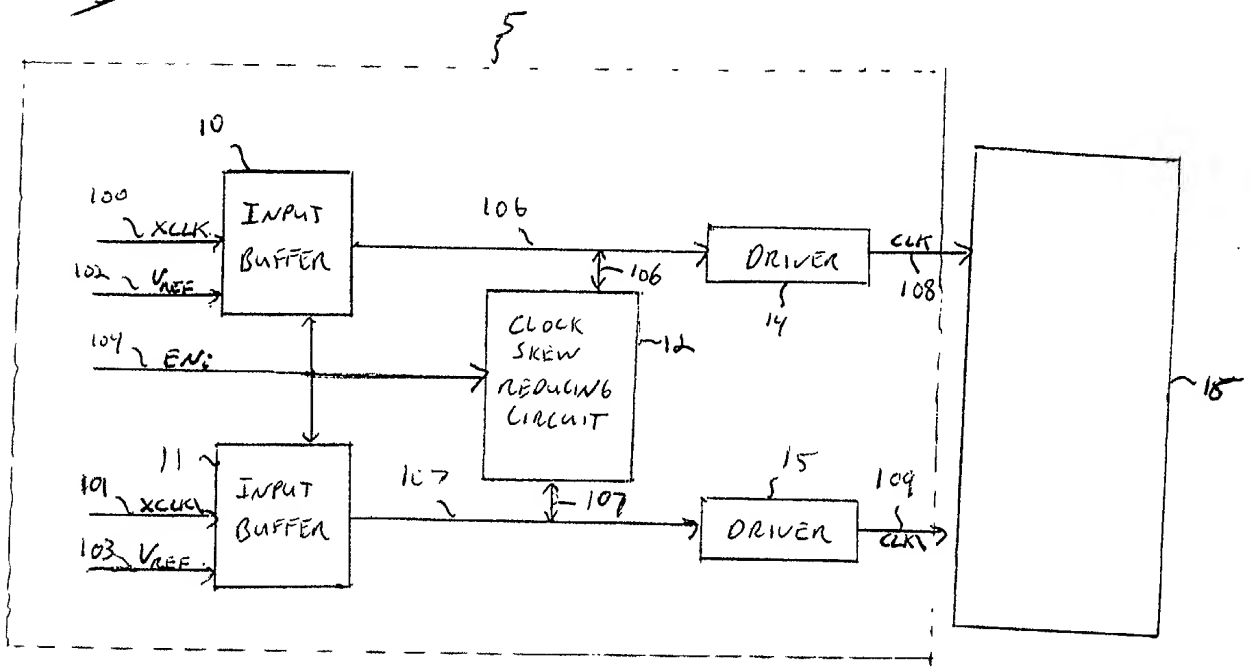


Fig. 2

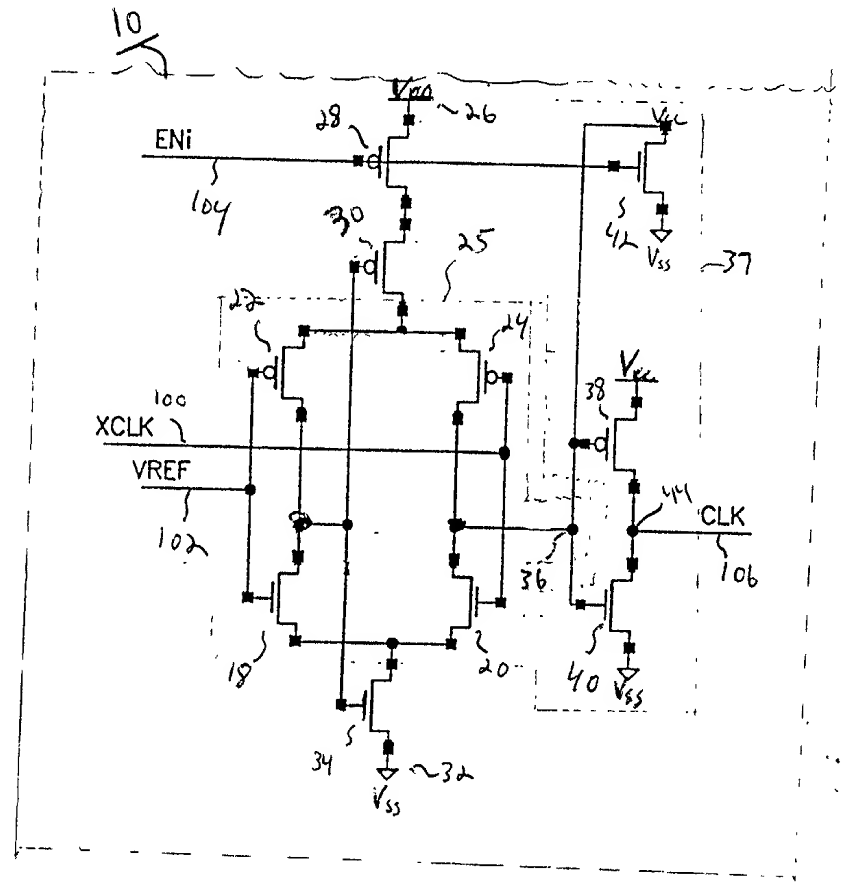


Fig. 3

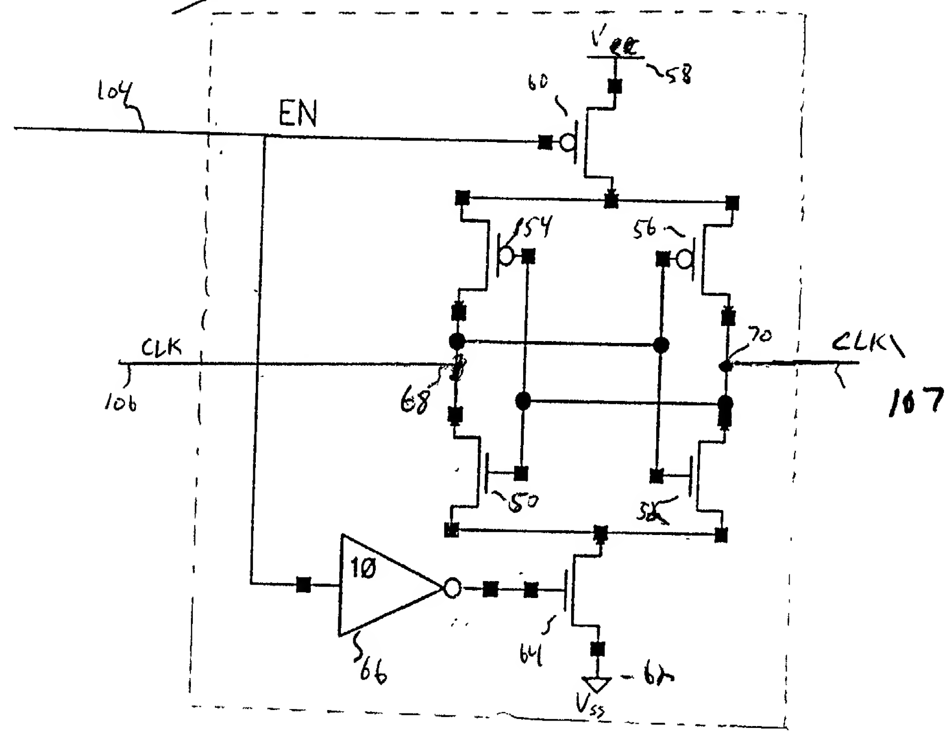


Fig. 4

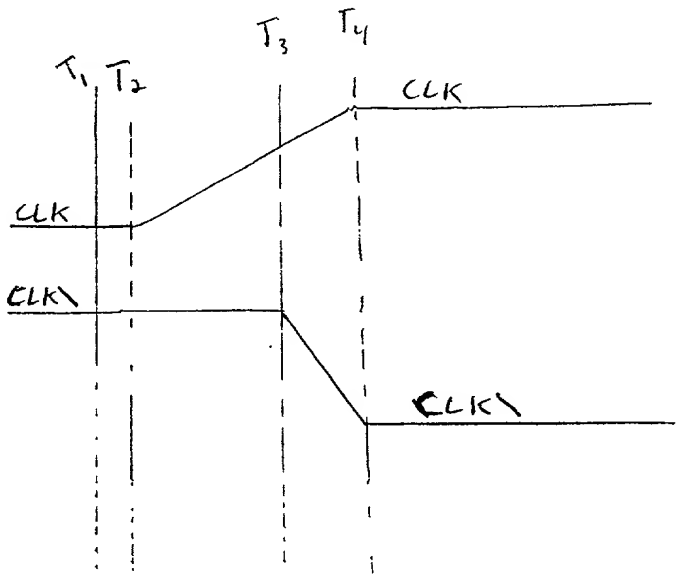


Fig. 5

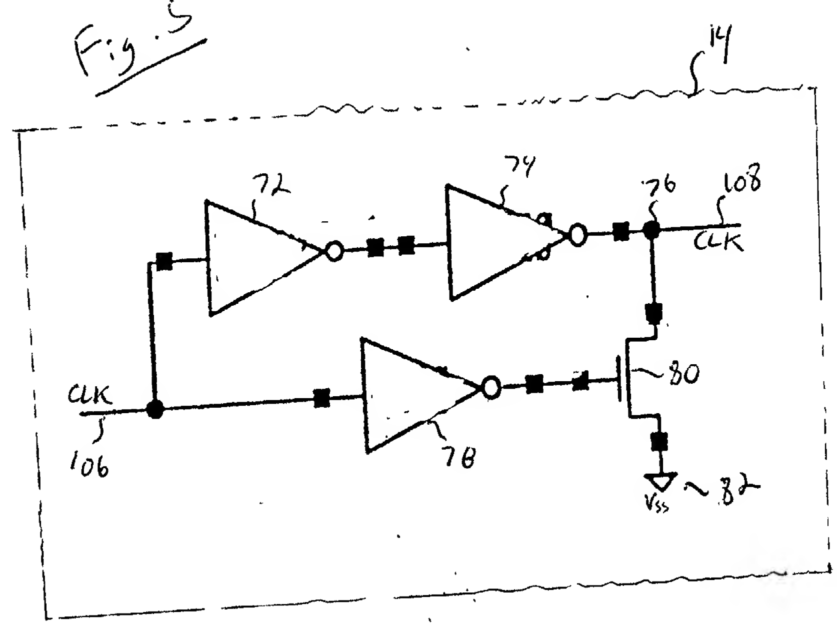


Fig. 6a

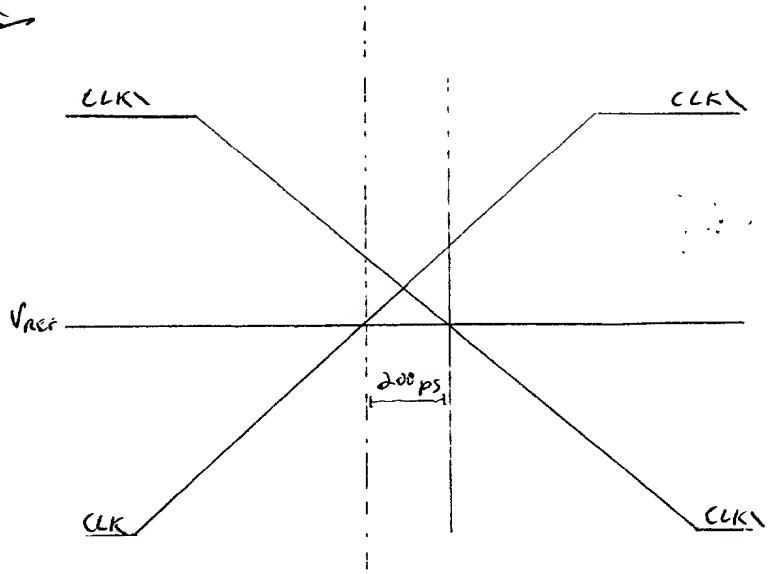


Fig. 6b

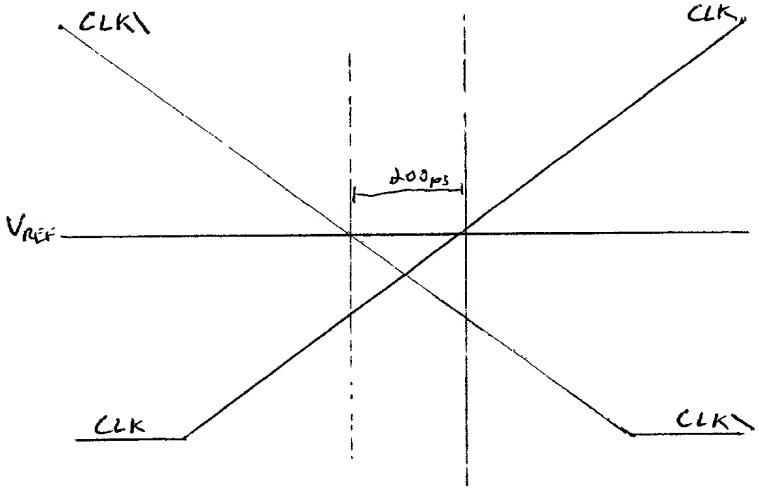


Fig. 6c

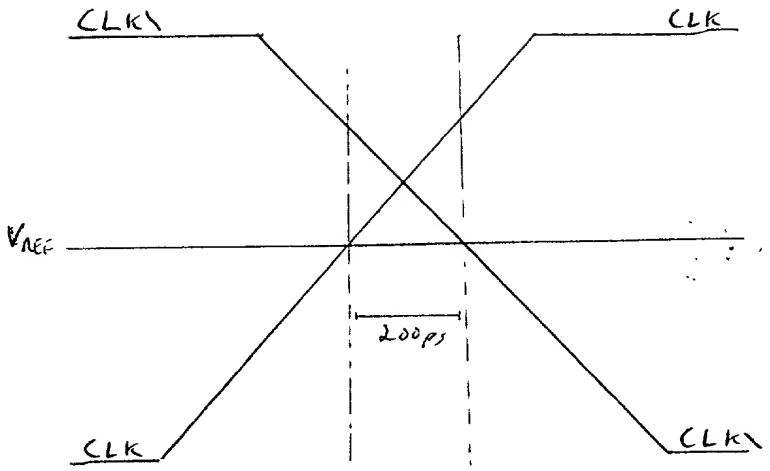
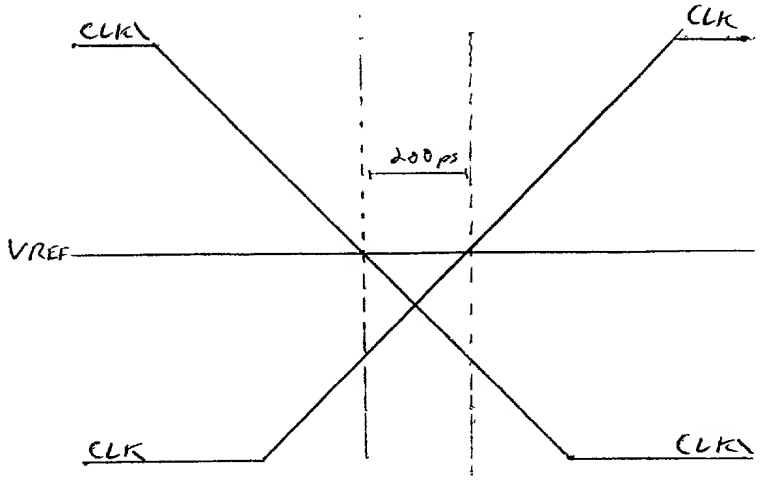


Fig. 6d



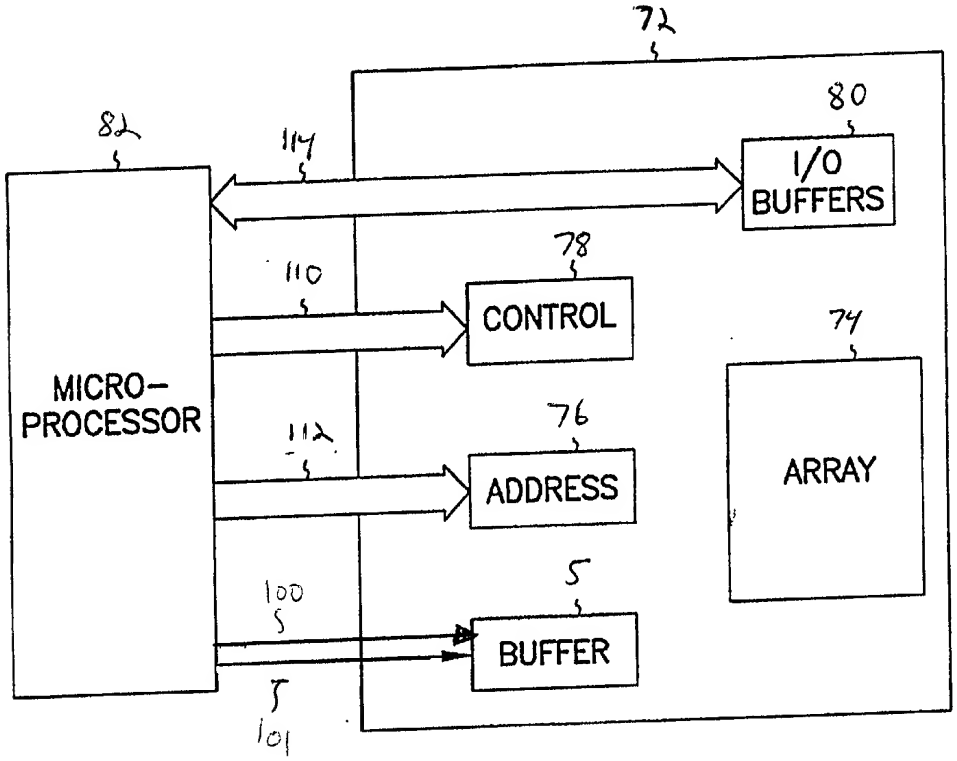


FIG. 7

Fig. 8

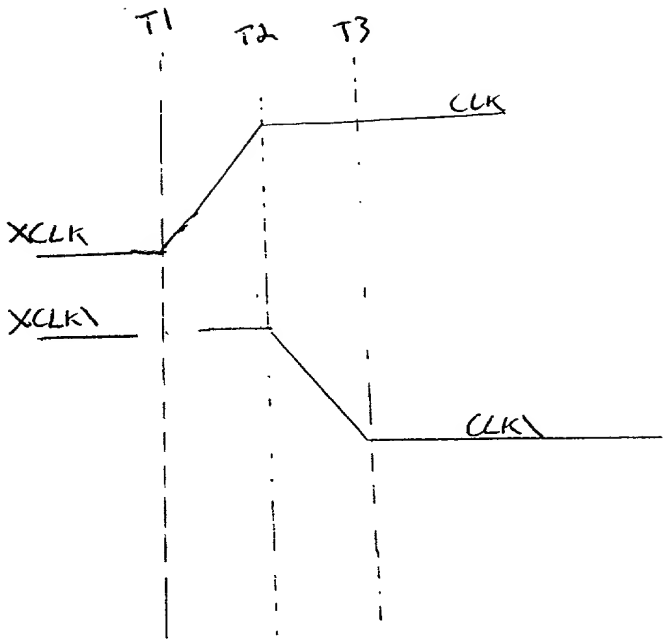


Fig. 9 PRIOR ART

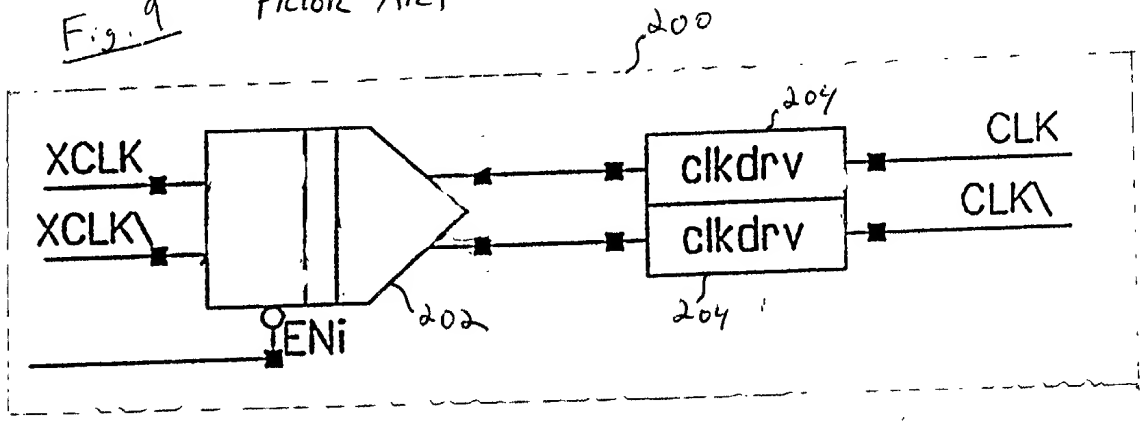


Fig. 10 PRIOR ART

CPU
Floppy Disk Drive
CD ROM Drive
I/O Device
I/O Device
Memory
ROM
118
82
124
126
116
120
72
122
150

Fig. 11

Docket No.: **M4065.0176/P176**
Micron No.: 99-0080

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject

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matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW, Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

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PATENT
Docket No.: M4065.0176/P176
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Christopher K. Morzano

Serial No.: Not yet Assigned

Group Art Unit: Not yet assigned

Filed: Herewith

Examiner: Not yet Assigned

For: APPARATUS AND METHOD FOR ADJUSTING CLOCK SKEW

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE AND

CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; Brian A. Lemm, P43,748; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; and James M. Silbermann, 40,413; and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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